REMARKS

By this amendment, Applicants have amended the claims to more clearly define their invention. In particular, Applicants have amended claim 32 to clarify, in the preamble, that the substrate is for semiconductor packages. Claim 32 has also been amended to recite that the wirings are formed on one side of the insulating supporting member, that the wirings comprise a predetermined wiring pattern including wire-bonding terminals, and that the substrate includes openings provided in the insulating supporting member at points where the external connection terminals are formed, reaching the external connection terminals. Claim 41 has been added to recite that the plural sets of wirings are formed only on one side of the insulating supporting member. The foregoing amendments are supported by, e.g., twelfth embodiment shown in Fig. 12 or the fifteenth embodiment shown in Fig. 17. See, especially, Figs. 12, 12, 17 and 17, and the description thereof in Applicants' specification. Claims 33, 34 and 38-40 have been cancelled without prejudice or disclaimer. Claims 35-37 have been amended to depend from 32.

In view of the cancellation of claims 33, 34 and 38-40, and the change in dependency of claims 36 and 37, the rejection of claims 33, 34 and 36-40, under 35 USC 102(e) as being anticipated by U.S. Patent No. 5,313,365 to Pennisi, et al. is moot. In any event, the Pennisi, et al. does not anticipate the presently claimed invention for the reasons set forth hereinafter.

Claim 32 stands rejected under 35 USC 103(a) as being unpatentable over Pennisi, et al. in view of U.S. Patent No. 4,602,271 to Dougherty, Jr., et al. Applicants traverse this rejection and request reconsideration thereof, at least insofar as it applies to the claims presently in the application.

The presently claimed invention relates to a substrate for semiconductor packages and to a semiconductor package produced, by, inter alia, mounting a semiconductor device on each a plural semiconductor device mounting regions of such a substrate. As set forth in amended claim 32, the substrate for semiconductor packages has an insulating supporting member and plural sets of wirings formed on one side of the insulating supporting member. The substrate also includes a semiconductor device mounting region and a resin-sealing semiconductor package region outside of the semiconductor device mounting region. The wirings comprise a predetermined wiring pattern including wire-bonding terminals and external connection terminals, the wire-bonding terminals being provided in the semiconductor package region and the external connection terminals being only within the semiconductor device mounting region. Openings are provided in the insulating supporting member at points where the external connection terminals are formed, reaching the external connection terminals.

The Pennisi, et al. patent discloses electronic packages for semiconductor devices and integrated circuits, in particular encapsulation of semiconductors directly attached to a circuit substrate. According to the encapsulated electronic package of Pennisi, et al., a printed circuit board is provided with a metal circuit pattern on one side. One or more semiconductor devices are attached to the printed circuit board with an adhesive, and covered by a glob top encapsulant. The glob top encapsulant also covers portions of the printed circuit board surface. The resin used to make the printed circuit board, adhesive and the encapsulant are an organosilicon polymer comprised substantially of alternating polycyclic hydrocarbon residues and cyclic polysiloxane or siloxysilane residues linked through carbon-silicon bonds. See column 2, lines 22-36. Note also column 3, lines 5-8 and 16-18.

On the other hand, the present invention has a structure where wirings including wire bonding terminals and external connection terminals are formed on one side of the insulating supporting member. In contrast, in Pennisi, et al., the metal circuit pattern 12 (which the Examiner apparently deems to be equivalent to the wire-bonding terminals of the present invention) are formed on the side on which the semiconductor devices are mounted on the board 11, while solder pads 27 (which the Examiner apparently deems to be equivalent to the external connection terminals of the present invention) are formed on another side of said board 11. Therefore, the structure of the printed circuit board 11 of Pennisi et al is completely different from the structure of the present invention since the structure of the printed circuit board 11 of Pennisi, et al. does not have wirings including wire bonding terminals and external connection terminals formed on one side of the insulating supporting member.

Furthermore, in the case of the present invention, openings are provided in the insulating supporting member at points where the external connection terminals are formed, reaching the external connection terminals. In contrast, the printed circuit board 11 of Pennisi, et al. does not have such openings.

The Pennisi, et al. patent discloses that the solder pads 27 are electrically connected to the integrated circuit die on the opposite side of the PCB, either by plated through holes or by blind vias (see lines 54-57 of column 4 of Pennisi, et al.). However, since, in the present invention, the external connection terminals and the wire-bonding terminals are formed on one side of the insulating supporting member, plated through holes or blind vias are not required.

The Dougherty, et al. patent discloses a package for semiconductor chips, wherein a substrate is provided with a repeating pattern of conductor ends, with each

pattern defining sites to permit the reception of a variety of different chips. The substrate of the described package is provided having a chip mounting surface, and is structured with conductors having opposite ends terminating at the mounting surface with intermediate portions connecting the ends of the conductors, the ends of the conductors being arranged in repeating patterns longitudinally along the substrate separated by orthogonal strips on the surface which are free of conductor ends to allow for dense surface wiring. The immediate portions of some conductors connected ends within a pattern and of some conductors connect ends in adjacent patterns. The conductor ends in each pattern are positioned to delineate a plurality of chip mounting sites having sufficient spacing between the conductor ends to permit the positioning of chip mounting means which may be electrically connected to the ends of the conductors by surface metallization. The substrate in Dougherty, et al. uses subsurface conductors to provide basic interconnection within each pattern and between adjacent patterns, and surface wiring for unique chip mounting and wiring. See from column 1, line 51 to column 2, line 9. Note also column 2, lines 38-45; and column 3, lines 4-6.

It is respectfully submitted that Dougherty, et al. discloses multiple levels of wiring in a vertical direction. It is respectfully submitted that Dougherty, et al., either alone or in combination with the teachings of Pennisi, et al., would have neither disclosed nor would have suggested such substrate or such package produced using such substrate, as in the present claims, including, inter alia, wherein the external connection terminals are provided only within the semiconductor device mounting region, wherein all of the external connection terminals are provided only inside of the wire bonding terminal, wherein plural sets of wirings are formed on one side of the insulating supporting member, and/or wherein openings are provided in

the insulating supporting member at points where the external connection terminals are formed, reaching the external connection terminals.

Moreover, it appears to be impossible to combine the substrate of Dougherty, et al. and the substrate of Pennisi, et al.; at the very least, there would have been no motivation to make the combination urged by the Examiner. Not only is there no motivation to combine these different types of substrate, the combined teachings would not have suggested the structure of the substrate of claim 32 by combining the substrate of Dougherty, et al. and the substrate of Pennisi, et al., because the characteristics of claim 32, such as, wirings including wire-bonding terminals and external connection terminals formed on one side of insulating supporting member are neither disclosed nor suggested in Pennisi, et al. or Dougherty, et al. Moreover openings reaching the external connection terminals formed on one side the insulating supporting member are neither disclosed nor suggested in Pennisi, et al. or Dougherty, et al.

For the foregoing reasons, the present claimed invention is patentable over the proposed combination of Pennisi, et al. and Dougherty, Jr., et al.

Claim 35 stands rejected under 35 USC 103(a) as being unpatentable over Pennisi, et al. as applied to claim 33, and further in view of JP 59-208756 to Katsuhiko. Applicants traverse this rejection, in at least insofar as it applies to the claims presently in the application.

The Examiner cites the Katsuhiko document as allegedly disclosing wire-bonding terminals comprising a nickel layer and a gold plate wire on its surface. However, it is submitted nothing in Katsuhiko would have remedied the basic deficiencies noted above with respect to Pennisi, et al. and/or the proposed

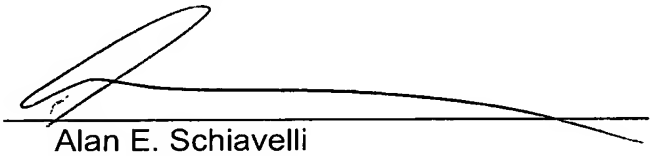
combination of Pennisi, et al. and Dougherty, Jr., et al. Accordingly, claim 35 is patentable for at least the reasons noted above.

In view of the foregoing comments and amendments, favorable reconsideration and allowance of all claims presently in the above-identified application are respectfully requested.

Applicants request any shortage in fees due in connection with the filing of this paper be charged to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (case 648.43481CC4), and credit any excess payment of fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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